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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/275,726	03/24/1999	BULENT DERVISOGLU	19705-000100	1134

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EXAMINER
TON, DAVID

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.	Applicant(s)
09/275,726	Dervisoglu et al.
Examiner	**Group Art Unit**
D. Ton	2133

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on 5/6/02 (Appeal Brief).

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-22 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 1-22 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☑ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

DETAILED ACTION

1. In view of the Appeal Brief filed on 5/06/02, PROSECUTION IS HEREBY REOPEN.

New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. The Final rejection (10/31/01) is withdrawn.

3. Claims 1-22 are presented for examination.

4. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

5. Gheewala(s) were cited as prior art in a previous Office Action.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-10 and 13-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Whetsel** patent no. **6,131,171**, in view of **Gheewala** patent no. **5,065,090**.

As per claim 1:

Whetsel teaches the invention substantially as claimed [see claim 1], including an integrated circuit IC 10 of Fig. 1] having logic blocks [see Fig. 2] comprising:

a control unit [TCR control 26 of Fig. 2] for performing test and debug operations of said logic blocks of said integrated circuit [see claim 1];

a memory [memory 30 of Fig. 2] associated with said control unit, said memory holding instructions for said control unit.

Whetsel teaches a plurality of lines [ODI of Fig. 1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1]. However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.

Gheewala teaches a cross-check test structure consists of a string of serial/parallel shift registers to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices [see Whetsel col. 4 line 54 - col. 5 line 13].

As per claims 2 and 5:

Whetsel teaches a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed to said integrated circuit [col. 4 lines 25-34].

As per claim 3:

Whetsel teaches the integrated circuit further comprising a unit [DBM of Fig. 2] coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

As per claims 4 and 6-9:

Gheewala teaches probes lines comprises a string of programmable connectors providing a signal path for carrying system operation signal at predetermined probe points of said logic blocks [Fig. 2].

As per claim 10:

Whetsel teaches the invention substantially as claimed, including an integrated circuit [IC 10, Fig. 1] comprising:

an interface [test port 38 of Fig. 2] for coupling to an external diagnostic processor;

a unit [TCR control 26 of Fig. 2] responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a memory [memory 30 of Fig. 2] coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit [test clock TCK of Fig. 1 and 2] so that said external diagnostic processor [external test bus controller 25 of Fig. 1, col. 3 lines 35-63] can process said capture system operation signals.

Whetsel teaches a plurality of lines [ODI of Fig. 1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1]. However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.

Gheewala teaches a cross-check test structure consists of a string of serial/parallel shift registers to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices [see Whetsel col. 4 line 54 - col. 5 line 13].

As per claims 13-14:

Gheewala teaches each of said probe lines comprises a string of programmable connectors operating at one or more clock rates [Fig. 4 and col. 8 lines 21-56].

As per claim 15:

Whetsel teaches the invention substantially as claimed, including a method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of lines of said logic blocks [see Fig. 1&2], said method comprising:

operating said logic blocks to perform normal system operations [see claim 1] at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said lines [ODI lines, col. 4 lines 41-68] responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving [col. 4 lines 41-68] said sets of system operation signals from said logic blocks along said lines at said system clock signal rates internal to said integrated circuit;

storing [claim 1] saids sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing [by an external tester, col. 1 lines 30-57] said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

Whetsel teaches a plurality of lines [ODI of Fig. 1&2] coupled to said control unit for carrying said system operation signals from predetermined points [data bus 16 of Fig. 1] of said integrated circuit to said memory [DBM of Fig. 1], wherein said lines providing signal paths from said point to said memory, said signal path capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signal stored in said memory so that said sets of system operation signal are retrievable [see col. 4 lines 41-68 and claim 1]. However, Whetsel does not explicitly teach the plurality of probe lines comprises strings of storage elements for carrying said system operation signals.

Gheewala teaches a cross-check test structure consists of a string of serial/parallel shift registers to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the ODI of Whetsel to include the probe lines comprising a string of storage elements as taught by Gheewala for carrying data signals from the data bus to the memory. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would enhance the test monitor operation to be controlled by the events detected over a range of DBM devices [see Whetsel col. 4 line 54 - col. 5 line 13].

As per claims 16-22:

Gheewala teaches each of said probe lines comprises a string of programmable connectors operating at one or more clock rates [Fig. 4 and col. 8 lines 21-56].

8. Claims 11-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Whetsel** patent no. **6,131,171**, in view of **Gheewala** patent no. **5,065,090** and further in view of **Gheewala et al**. patent no. **5,202,624**.

As per claims 11 and 12:

Whetsel and Gheewala (5,065,090) do not teach an IC including a trigger logic.

Gheewala et al. (5,202,624) teaches a trigger logic [see circuitry of Fig. 3 and the logic of TABLE A on col. 6 and TABLE B on col. 8] responsive to said system operation signals for initiating/terminating storage of said system operation signals in said memory [when P1=0 and P2=0, S2 value is written into latch 68, when control signal C=1, the value then transmitted to driver 42, col. 7 lines 1-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Whetsel and Gheewala to include a trigger logic for initiating/terminating storage of said system operation signals in said memory as taught by Gheewala because it would provide the advantages that the test signals are loaded to internal probe points without the need for complex scan registers [see Gheewala et al. col. 2 lines 42-57].

Response to Arguments

9. Applicant argues that the prior art of record do not teach the handling of "system operation signals".

The newly cited art, Whetsel, teaches a digital bus monitor (DBM) which is used to observe and test the bus in normal operating speeds [claim 1]. Another word, Whetsel teaches a test system for handling of "system operation signals" during normal operating speeds.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 746-7239 (Official)

(703) 746-7240 (Non-Official)

(703) 746-7238 (After-Final)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

dt

January 06, 2003

DAVID TON
PRIMARY EXAMINER